Hall Ticket Number:

Code No.: 6201M

VASAVI COLLEGE OF ENGINEERING *(Autonomous)*, HYDERABAD
M.E. I Year (ECE) II-Semester (Make Up) Examinations, Sept./Oct.- 2015
(Embedded Systems and VLSI Design)

Mixed Signal IC Design

Time: 3 hours Max. Marks: **70**

*Note: Answer **ALL** questions in **Part-A** and any **FIVE** questions from **Part-B***

Part-A (10 X 2=20 Marks)

1. Explain how analog and digital operations are performed by the same circuit. What are such circuits called?
2. Calculate the equivalent resistance of a 5pF capacitance sampled at a clock frequency of 100 KHz.
3. Discuss the problems that arise in integrating analog and digital circuits on the same substrate.
4. Describe the operation of a non inverting discrete time integrator working on two clock phases.
5. Explain aperture jitter in a Sample and Hold circuit.
6. Suggest a circuit for Sample and Hold operation used to minimize slewing time.
7. Define resolution and differential non linearity (DNL) of a data converter.
8. An ideal 10-bit unipolar Digital to Analog converter has V_{LSB} = 1mV. What is the largest output?
9. Discuss the advantages of oversampled converters over Nyquist converters.
10. Define Lock range and Capture range of a PLL.

Part-B (5 X 10=50 Marks)

11. a) What is a voltage comparator? Explain the operation of an op-Amp based comparator. [6]
    b) Mention the basic building blocks of a switched capacitor resistor. [4]

12. a) Give the architecture of a switched capacitor low pass first order filter. [4]
    b) Suggest one method to minimize the charge injection error in a switched capacitor comparator. [6]

13. a) With a neat circuit diagram explain the transmission gate Sample and Hold circuit. Draw the output waveforms. What are the advantages of using transmission gate in the circuit? [6]
    b) Discuss quantization noise connected with ADCs. [4]

14. a) Explain VCO based Analog to Digital converter. Compare its performance with flash ADC. [5]
    b) Explain thermometer code converter. [5]

15. a) A 1-bit A/D oversampled converter has 6 dB SNR. What sample rate is required using oversampling (no noise shaping) if f_o = 25 KHz? [4]
    b) Explain an oversampled A/D converter without noise shaping. [6]

16. a) A type I PLL experiences a frequency step $\Delta\omega$ at t = 0. Calculate the change in the phase error. [4]
    b) Explain the operation of a charge pump PLL. [6]

17. Write short notes on any **two** of the following:
    a) Latched comparator [5]
    b) Diode bridge based Sample and Hold circuits [5]
    c) Cyclic A/D converter [5]

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